forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode;

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor; and

incorporating said multi-region planar thyristor in a memory device.

55. (Twice Amended) A method of forming a device for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode, said gate adapted to receive a voltage for producing latch-up in said multi-region planar thyristor; and

incorporating said multi-region planar thyristor in a memory device.

62. (Once Amended) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; and

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor and to a write row address line of a memory integrated circuit, said thyristor being adapted to transition from a first one to a second one of said at least two possible current states.

Please add new claim 63-65 as follows:

63. (New) A method of forming a memory integrated circuit comprising:

forming a plurality of thyristor structures over a substrate;

forming a plurality of gates disposed over respective single junctions of said plurality of thyristor structures;

forming a plurality of channels disposed between said thyristor structures, whereby said thyristor structures are disposed in spaced relation to one another; and

mutually coupling at least two gates of said plurality of gates to a write row address line of said memory integrated circuit.

64. (New) A method of forming a circuit for storing information as one of at least two possible stable current states as defined in claim 48 wherein said incorporating said multi-region planar thyristor in a memory device comprises coupling said at least one polysilicon gate to a write row address line of said memory device.

65. (New) A method of forming a device for storing information as one of at least two possible stable current states as defined in claim 55 wherein said incorporating said multi-region planar thyristor in a memory device comprises coupling said at least one polysilicon gate to a write row address line of said memory device.